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# APPLICATION FOR UNITED STATES PATENT

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**Title:** INTEGRATED ELECTROSTATIC INDUCTIVE COUPLING  
FOR PLASMA PROCESSING

## SPECIFICATION

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**INTEGRATED ELECTROSTATIC INDUCTIVE COUPLING  
FOR PLASMA PROCESSING**

[0001] This invention relates to high density plasma generating devices, systems and processes, particularly for the manufacture of semiconductor wafers. This invention particularly relates to the high density inductively coupled plasma sources with slotted deposition baffles and RF biased wafer supports used in semiconductor processing.

**Background of the Invention**

[0002] There are two principal groups of the plasma sources: capacitively-coupled plasma sources, which utilize RF electric field coupling to the plasma, and inductively coupled plasma (ICP) sources, which utilizing RF magnetic field coupling to the plasma.

[0003] Capacitively-coupled plasma sources include "planar diode" or "parallel plate" systems, in which a surface to be etched is placed on one electrode that is coupled to an RF generator through a blocking capacitor, which does not allow real current to flow from the electrode to the RF generator. This forces the plasma to find a condition in which the electron current reaching the electrode from the plasma must exactly balance

the ion current averaged over one RF cycle. Since electrons are more mobile than ions, the electrode must acquire a negative potential to limit the electron current and encourage the positive ion current. This negative potential is called the self-biased voltage, which results in an energetic ion bombardment of the surface being etched. Changing applied RF power can control the ion bombardment. A planar triode capacitively-coupled plasma system with two RF electrodes and grounded walls represents another geometry.

[0004] Capacitively-coupled sources have widespread use in semiconductor plasma processing, but have some problems and limitations. For instance, the electrical behavior of a capacitively-coupled discharge is influenced by the reactor geometry, where plasma potential depends strongly on the area of the powered electrode relative to the area of all other surfaces in contact with the discharge. In symmetrical systems, both electrodes can be subjected to high-energy ion bombardment, including energetic ion bombardment of walls and fixtures causing sputtering of these surfaces and chamber contamination. The pressures typically used have to be maintained high enough ( $> 100$  mTorr) so that sputtering of the grounded surfaces is not a problem. In asymmetric systems, low energy ions move toward the walls, which causes a nonuniform plasma density that peaks in the center. Non-uniform plasma caused by large losses of electrons and ions to the chamber walls causes nonuniform etch rates to result. Optimal geometry at low pressure has been cylindrical geometry, which is not adaptable to 300 mm single wafer semiconductor equipment manufacturing.

[0005] A common drawback of the above-described systems is an inability to independently control ion energy and ion flux at a fixed pressure and RF frequency. Planar triode systems solve this problem but require relatively high pressure to eliminate sputtering of the top electrode, which voltage can be reduced by increasing frequency at

the top electrode and decreasing frequency at the wafer electrode. In the VHF frequency range, high plasma densities can be generated with low applied voltages. Higher frequencies result in less damage, more uniformity across the electrode, and the ability to process larger substrate areas at more uniform rates.

[0006] Inductively coupled plasma (ICP) sources provide relatively low ion energy bombardment and reasonable etch rates. Common ICP sources include coils having planar, cylindrical or dome-shaped geometries. The so-called helical resonator is a cylindrical ICP source in which a movable tap on the coil is used to optimize tuning and power transfer into the plasma. The helicon source is an ICP source that uses an antenna with specific geometry to launch a wave along an externally applied magnetic field and this wave can couple energy into the plasma electrons. High frequency (2.45 GHz) electromagnetic radiation is also used to generate high-density plasma in microwave range excitation but is limited to  $< 10^{11}$  electrons per  $\text{cm}^3$ , and mostly used as downstream plasma for wafer processing. In combination with large magnetic fields (875 Gauss for excitation at 2.45 GHz) an electron cyclotron resonance condition (ECR) can be found with which plasma densities in the  $10^{13} \text{ cm}^{-3}$  range can be achieved. There are many commercially available plasma sources that can be used to generate high-density plasmas ( $>10^{11}$  electrons  $\text{cm}^{-3}$ ) at relatively low pressures ( $<10$  mTorr) without requiring the application of high voltages.

[0007] Plasma sources are used in combination with a capacitively-coupled, RF-powered electrode on which the processed wafer is placed. Such an electrode is often an electrostatic chuck (ESC), which consists of a base plate mounted having cooling channels and/or heating structure inside and connections for backside gas, DC chucking electrodes, and temperature detectors, etc. In some cases a flexible bellows mounted

between a robust backside flange and a bottom chamber flange allows vertical movement of the ESC to enhance process control variables.

**[0008]** In systems with independently RF biased substrate holders, independent control of the ion energy and ion flux can be obtained. Typically, the power used in the high-density plasma source is much larger than the bias power applied to the wafer-bearing electrode. Increasing the bias power increases the ion energy without changing the ion current density. Increasing the source power results in both an increase in the ion flux and a decrease in the ion energy.

**[0009]** Etch uniformity at the wafer is affected by ion flux and ion energy. Generally, the ion flux towards the wafer is a function of plasma density distribution. To achieve uniform etching, uniformly distributed plasma parameters have to be provided. Typically, the ICP sources with a spiral coil produces a plasma distribution with a peak in its center. Multiple coil configurations, magnetic fields, wafer pedestal size and material and additional chamber hardware are used to improve plasma density distribution. For instance, multipolar magnetic field confinement of a plasma helps to increase plasma density and improved plasma homogeneity, however only for pressures well below 1 mTorr. At higher pressures, the plasma homogeneity degrades rapidly as the pressure is increased. Another solution has implemented a magnetic confinement ring around an electrostatic chuck to confine the plasma within the area defined by the ring. Unfortunately, the magnetic confinement ring often produces the well-known cusp effect on the peripheral surface of the wafer due to the magnetic field of the confinement ring.

**[0010]** In ICP systems, the use of dual coils or dual zone coil configurations within an ICP source partially improves the plasma density distribution. However, because of the distance of the coil from the wafer pedestal, increased RF power is

required to compensate radial power loss, e.g. an additional RF generator and matching unit are typically needed. Still, the sidewall effect is not removed definitively from the wafer. Significant chamber modifications may be required, larger size dielectric windows may be needed, the window should be thick enough to withstand atmospheric forces, and additional controlling units and cooling are required. For current 300 mm size wafers, all these components represent large and expensive consumable parts, increased complexity, resulting in high cost of operation (COO) and significantly high overall cost of the machine.

[0011] Furthermore, producing uniformly distributed plasma over a wafer may have the undesirable effect of reducing plasma density. A wafer exposed to the reduced plasma density generally takes more time to produce a desired etch or deposition than a wafer subject to a higher plasma density. Hence, the etch or deposition process may take longer to complete in a uniformly distributed plasma environment.

[0012] Accordingly, there is a need for an ICP source that produces a high density uniform plasma that is simple and low in cost.

### **Summary of the Invention**

[0013] An objective of the present invention is to provide a plasma source for utilization in a plasma process, such as plasma etching, plasma deposition or plasma cleaning, that is uniform across the surface of the substrate being processed. Another objective of the invention is to provide a compact plasma source that can be used either as primary plasma source or as complementary source to a primary ICP source. A further objective of the invention is to provide a highly effective plasma source for a simplified reduced cost chamber.

**[0014]** According to principles of the present invention, an integrated, electrostatic, inductively-coupled wafer support (i-ESIC) is provided in the vacuum chamber of a plasma processing apparatus. The i-ESIC wafer support has two integrated portions, including a central wafer support surface that is capacitively coupling to the plasma, and an inductive ionization source that is connected to the central surface and provides inductively-coupled RF energy to the plasma.

**[0015]** In the illustrated embodiment, the capacitively-coupled central wafer support surface is an electrostatic chuck (ESC), which holds a wafer during processing. The chuck is preferably biased to a negative potential relative to the plasma to control the energy of ions from the plasma onto the supported substrate. The inductively-coupled component is preferably annular and surrounds the central portion, coupling energy to the plasma through RF magnetic fields generated by an inductive element therein.

**[0016]** In the preferred embodiment, the central substrate support surface and the annular inductive element are coupled in series between the chamber ground and an RF generator through a matching network. For example, the central support may be capacitively-coupled to the matching network and capacitively-coupled to the inductive element, which, in turn, may be capacitively-coupled to ground. The impedances of the series circuit may be designed in conjunction with those of the matching network to produce a single resonant circuit. Alternative configurations are described below.

**[0017]** According to certain principles of the present invention, the integrated wafer chuck and active peripheral ionization source is provided. With the source, plasma is generated in the vicinity of the wafer where it will affect immediately the plasma distribution above the wafer. Because of the close proximity of the source to the wafer, the source does not require a large RF power supply. The source may be used as a

secondary or complementary source with which plasma is generated that compensates for non-uniformity generated by a primary ICP source. The source of the present invention generates a higher density plasma that diffuses into a low-density capacitively-coupled plasma above the wafer. With the present invention, RF hardware can be reduced in size and power. The source may be used as a single integrated plasma source sufficient to process wafers placed on the pedestal, which may be, for example, an electrostatic chuck (ESC).

[0018] The present invention is based, in part, on the principles that etch uniformity at a wafer is affected by plasma density distribution and by ion energy, and that to achieve uniform etching, uniformly distributed plasma parameters should be provided. It has been found that it is not sufficient to reduce the loss to the walls only in a passive way, and that the most effective way to reduce loss to the walls is to generate an active plasma in the depleted region around the wafer. Plasma density above the wafer is most easily affected by plasma generation in the vicinity of the wafer. This is done by using ICP, which leads to high-density plasma generation. This approach does not require oversized RF power supplies. The present invention utilizes existing RF generators to bias a wafer pedestal. A center-peaked plasma distribution that is generated by the remote primary ICP source may be compensated for at the wafer edge by peripheral plasma generation from a secondary high-density plasma source according to the present invention.

[0019] These and other objectives and advantages of the present invention will be more readily apparent from the following detailed description.



**Brief Description of the Drawings**

[0020] **Fig. 1** is a diagrammatic cross-sectional view of a plasma processing apparatus embodying principles of the present invention.

[0021] **Fig. 2** is a perspective diagram, partially cut away, illustrating one embodiment of an integrated, electrostatic, inductively-coupled wafer support of the apparatus of **Fig. 1**, according to one embodiment of the invention.

[0022] **Fig. 2A** is an enlarged perspective view of a portion of one embodiment of a shield of the integrated, electrostatic, inductively-coupled wafer support of **Fig. 2**.

[0023] **Figs. 3A-3F** are cross-sectional diagrams of six exemplary coils that can be used for the inductively-coupled element of the wafer supports of **Figs. 1** and **2**.

[0024] **Figs. 4A-4B** are top and perspective diagrams, respectively, of one embodiment of a bifilar coil similar to that of **Fig. 3F**.

[0025] **Figs. 4C-4D** are top and perspective diagrams, respectively, similar to **Figs. 4A-4B**, of another embodiment of a bifilar coil.

[0026] **Figs. 5A-5C** are perspective diagrams of one embodiment of an inductive element, a graph of time-averaged RF electromagnetic energy for such element, and a graph of power density delivered into the plasma by such element.

[0027] **Figs. 6A-6B** are top and perspective diagrams, respectively, of another embodiment of an inductive element for the wafer support of **Figs. 1** and **2**.

[0028] **Fig. 6C** is a graph of time-averaged RF electromagnetic energy for the element of **Figs. 6A** and **6B**.

[0029] **Fig. 6D**, is a slot pattern diagram for a Faraday shield for use with the element of **Figs. 6A** and **6B**.

[0030] **Fig. 6E** is a graph of time-averaged RF electromagnetic energy for the element of **Figs. 6A** and **6B** equipped with a Faraday shield having the slot pattern of **Fig. 6D**.

[0031] **Fig. 7** is a disassembled perspective view of an alternative embodiment of the wafer support of **Figs. 1** and **2** that employs a segmented peripheral source for the inductive element.

#### **Detailed Description**

[0032] As illustrated in **Fig. 1**, according to one embodiment of the invention, a plasma processing apparatus 10 includes a vacuum processing chamber 11 enclosed in a chamber wall 12. An integrated, electrostatic inductively-coupled device or wafer support (i-ESIC) 20 is mounted in the chamber 11 to support individual wafers 14 thereon for processing by a plasma 15 maintained within the vacuum chamber 11.

[0033] Referring to **Figs. 1** and **2**, the wafer support 20 has two integrated main components or portions: a capacitive-coupling component 21, which provides a capacitively-coupled RF path to a plasma 15, and an inductively-coupled component 22, which provides an inductively-coupled RF path to the plasma 15. The capacitively-coupled component 21 is a central substrate support portion, typically an electrostatic chuck (ESC), which holds individual wafers to the support 20 during processing. The chuck of the central portion 21 also provides control of the energy of ions from the plasma by capacitively coupling RF power to the plasma 15 and generating a voltage bias on the wafer 14 with respect to the plasma potential. The inductively-coupled component 22 is annular and surrounds the central portion 21, providing coupling to the plasma

through RF magnetic fields generated by an inductive element incorporated within annular portion 22.

**[0034]** The i-ESIC wafer support 20 is compact and includes the central portion 21 and the perimeter portion 22. The central portion 21 of the substrate support 20 serves as a support for a wafer 14, holding and releasing wafers according to principles known in the field of ESC manufacturing and applications. The central portion 21 contains heating/cooling devices (not shown) to sustain wafers 14 at process temperature, and other sensors and instrumentation (also not shown) used in such devices. Internal structure of the ESC is well known to those familiar with the field. The substrate support 20 is biased through a capacitor 16 and a matching network 17, which are connected in series between the support 20 and an RF power supply 18.

**[0035]** The peripheral portion 22 has an inside diameter that is larger than the diameter of the wafers 14 that are to be processed on the support 20. Peripheral portion 22 includes an annular inductive device 23 having an inner end 23a connected through an impedance 24 to the central portion 21, and an outer end 23b connected through an impedance 25 to a bottom chamber shield and support flange 26, which is grounded via the chamber walls 12. The central portion 21 is supported on, and insulated from, the support flange 26 by an insulator ring 31. The inductive device 23 has a relatively low inductance (less than 1 micro-Henry) and is schematically shown in **Fig. 1** supported on the support 20 in an insulating envelope 27, formed of  $\text{Al}_2\text{O}_3$  or other suitable dielectric, which insulates the inductive device 23 from the bottom shield 26. The grounded bottom shield 26 electrically shields the device 20 to prevent plasma ignition below the support 20.

[0036] The top surface 23c of the inductive element 23 is protected from the plasma 15 by a metallic shield 28. Shield 28 serves as a Faraday shield and is made of an electrically high-conductivity material such as metal. To provide transparency to RF magnetic fields, the shield 28 contains radially or almost radially extending slots 29 that overlap the width of the inductive element 23. Generally, the slots 29 of the shield 28 are oriented in parallel or almost parallel to the flux lines of the RF magnetic field generated by the inductive element 23. The number and dimensions of the slots 29 are not critical and can vary, but a relatively low number of slots will provide operation of inductive device 23 as an ICP source in an ICP mode. To achieve good azimuthal uniformity, a minimal number of slots should be at least  $N \geq \pi / (2 \arctan (d/2D))$ , where  $d$  is the width of the annular inductive element 23 and  $D$  is the diameter of an annular inductive element 23. In the illustrated embodiments,  $N$  is approximately 12. Above a certain number of slots, for example 60 to 80, which might exist for inductive elements 23 having diameters of from 300 to 400 mm, the performance of the element 23 as an ICP source is not strongly affected by increasing the number of slots 29. Typical and preferable slot width is in the range of 0.5-5 mm, although the acceptable range of slot width is not limited by this interval.

[0037] The electrostatic shield 28 functions to protect the inductive element 23 from the plasma 15, (e.g. from the direct heating, erosion, sputtering of the surface, contamination or conductive deposits) and to provide effective ICP operation. One example of a preferred configuration of slots 29 for the shield 28 is shown in the **Fig. 2A**. Overlapping portions 29a of the slot structure eliminate direct deposition on the inductive element 23. Other slot configurations, such as slots 29 of chevron-shaped cross-section, might also be preferable.

**[0038]** As described and illustrated above, the wafer support 20, together with inductive device 23, is compact. The inductively-coupled member 22 of the support 20 provides increased density at the perimeter of the wafer 14, and thus compensates for radial loss of charged particles towards the walls 12 of the chamber 11, and generates plasma 15 of uniform density above the wafer 14 being processed. The i-ESIC device operates continuously in two modes: a capacitive-coupled plasma (CCP) mode in the center of the device 20 where the wafer 14 is supported, and an inductively-coupled plasma (ICP) mode at the perimeter of the wafer 14, both modes being powered utilizing a common matching network 17 and RF generator 18.

**[0039]** In operation, the chamber 11 is under vacuum, e.g. pumped to a base pressure and filled with processing gas at low pressure, typically, but not necessarily, in the range of from several mTorr to 100 mTorr. With no plasma inside the chamber, RF power from the RF generator 18 through matching network 17 and capacitor 16 is delivered to the substrate holder 20. Before plasma is ignited, RF current cannot flow through the high impedance low-pressure gas. The substrate holder 20, which is connected to an inductive element 23 in series with the impedances 24 and 25 and eventually, including stray capacitance, to ground, produces a serial resonant circuit that includes the capacitor 16 at the output of the matching network 17. Resonant frequency of such serial resonant circuit  $f$  is given by  $f=1/(2\pi\sqrt{LC})$ , where the capacitance  $C$  in series with the inductive element 23 includes all of the capacitances of the circuit.

**[0040]** The inductive element 23 itself, due to stray (mutual) capacitances, represents a serial-parallel resonant circuit. Portions of the parallel capacitive component of the parallel resonant circuit of the inductive element are formed from the distributed

inter-winding capacitances of the inductive element 23, while other stray capacitance is from the element 23 to ground. A rough estimate for a typical single helical or spiral coil (3 - 4 turns, diameter from 100 to 400 mm) of a type used in plasma processing gives a resonant frequency approximately in range from about 1 MHz to 100 MHz.

[0041] Under vacuum conditions, in the serial circuit loop the resistance is very small (e.g. the Q-factor of such resonant circuit is very high). At resonant conditions the impedance of inductive element 23 is high so an induced voltage at the inductive element will be high. Because the antenna end connected to substrate holder through impedance 24 is at a higher potential than the end connected to the ground through impedance 25, an intense electric field will ignite the plasma 15 within low pressure processing zone of the chamber 11. Generally, the matching network 17 does not need to match absolutely into the parallel resonance frequency, because the inner end of the inductive element that is connected through impedance 24 to central portion 21 of the wafer holder 20 can strike plasma by capacitive coupling more easily than the inductively-coupled component 22. Relatively low power (<100 Watts) is sufficient to ignite plasma by capacitive coupling.

[0042] Once the plasma 15 is ignited, it spreads into the volume of the chamber 11 above the inductive element 22, where an intense electric field induced by the RF magnetic field will deliver additional RF power into the plasma 15. The load that the inductive element 23 now sees is much larger. The inductive element 23 is thereby coupled to a resistive plasma 15. Increased resistive load in series in loop with inductive element 23 lowers the Q-factor of resonant circuit, which reduces the voltage on the inductive element 23. Matching to the new resonance frequency increases the current through inductive element 23.

[0043] Because the substrate holder 20 is exposed now to the plasma 15, RF current flows through the wafer 14 and a capacitive sheath into the plasma 15, creating a parallel loop to the inductive element loop. This creates a parallel resonant circuit with capacitance given by the ESC 21, wafer 14 and sheath capacitances.

[0044] At constant plasma parameters, e.g. when process parameters are optimized for unique process conditions, the choices among the inductive element inductance and the various capacitances may provide resonance at the same excitation frequency as the RF supply 18. Then there would be no need for tuneable matching network. However, a high impedance RF power supply should be used in such case or at least a load capacitor should be used to set the impedance of the mismatched line due to varying coil impedance at vacuum and plasma conditions, and to reduce any mismatch due to varying plasma parameters.

[0045] The inner impedance 24 may be omitted; however, at very low pressure it eliminates self-DC bias of the inductive element 23 by potential from the ESC 21, thus eliminating arcing. Similarly, the outer impedance 25 may be omitted; however, it provides a more convenient distribution of the RF potential on the inductive element 23 to reduce arcing probability.

[0046] In some special cases, for example, bifilar antenna configurations, the value of the stray capacitance of the inductor 23 can be designed into the inductive element 23, as can the capacitances in and out of the inductor through impedances 24 and 25, either one or both of which can be replaced by such stray capacitance or otherwise integrated into the device in the form of dielectric coatings deposited between the capacitive substrate holder portion 21 and the inductive element 23 of the peripheral inductive portion 22. The thickness of these coatings and cross-sectional areas of the

metallic parts at the end connections define the values of the various capacitances. Typically, the surface of the electrostatic chuck is coated by sprayed Alumina. Other dielectric materials or their combinations may be used.

[0047] Overall, several relations, which are practical and may be used as the design rules in the development of the I-ESIC device. The inductance  $L_{ANTENNA}$  and parallel capacitance  $C_{PARALLEL}$  of the inductive element 23 should be within range  $C_{PARALLEL} \cong \beta (1 / \omega^2 L_{ANTENNA})$ ,  $0 < \beta < 1$ . The effective inductive impedance of the inductive element is then estimated by inductance  $L_{EFFECTIVE\ ANTENNA} \cong L_{ANTENNA} / (1 - \beta)$ ,  $0 < \beta < 1$ . The relation of the capacitance in series with inductive element 23 is  $C_{PARALLEL} \cong (1 - \beta) / (\gamma \omega^2 L_{ANTENNA})$ ,  $0 < \beta < 1$ ,  $0 < \gamma < 1$ . Accordingly, the effective impedance of the ICP branch,  $L_{EFFECTIVE\ ICP}$ , (the inductively-coupled portion 22 of the support 20), is within the range  $L_{EFFECTIVE\ ICP} \cong L_{ANTENNA} (1 - \gamma) / (1 - \beta)$ ,  $0 < \beta < 1$ ,  $0 < \gamma < 1$ ; and the impedance of the CCP branch,  $C_{CCP}$  (the capacitively-coupled portion 21 of the support 20) is within the range  $C_{CCP} \cong (1 - \beta) / ((1 - \gamma) \omega^2 L_{ANTENNA})$ ,  $0 < \beta < 1$ ,  $0 < \gamma < 1$ .

[0048] In accordance with another embodiment of the invention, the RF signal from the matching unit 17 may be supplied to the outer end of the inductive element 23 through the impedance 25, and the inductance 23 connected through impedance 24 to the substrate holder 21. In this case when igniting plasma, instead of a parallel resonant circuit, the serial resonant circuit will remain. However, the resonant frequency will change due to the change in serial capacitance to the inductive element 23.

[0049] Still another embodiment disclosed in this invention integrates the inductive element 23 within the matching network 17, with the inductive element 23 and impedances 24 and 25 replacing the coil of the matching network between the connection



points of adjustable load and tuning capacitors connected to ground (not shown). This makes a very compact integrated ESIC.

[0050] The design and construction of the matching circuits 17 are well known to persons skilled in the art. In general, an RF matching unit 17 includes several variable reactive elements (inductors or capacitors) by which the impedance of the RF matching section can be adjusted to achieve a match between RF cable (or nominal RF generator output) and an RF driven electrode or coil to thereby maximize the RF power that is delivered to the plasma 15 within the chamber 11. A combination of the series and parallel elements can result in the desired impedance match of the source inductor to the driving generator for maximum current. Generally, three elements can be used to match any discharge and inductive element impedances.

[0051] The inductive element 23 may have single or multiple turns that can be connected in parallel or in series. Several examples are shown in **Figs. 3A-3F**, but disclosure is not limited by these only. In each of these figures, the wafer support 20 is shown made up of the capacitively-coupled component or ESC 21 and the inductively-coupled component 22 coupled together in series resonant circuit. The inductively-coupled component 22 is, in turn, made up of the inductive element 23 coupled in the series circuit between the impedances, typically capacitances, 24 and 25. Each figure shows the matching network output connected to the ESC 21. The inductive element 23 is a planar two-turn concentric coil in **Fig. 3A**, a conical concentric coil in **Fig. 3B**, a cylindrical or helical coil in **Fig. 3C**, combined concentric coils in **Fig. 3D**, a two-planar concentric coil in **Fig. 3E**, and a bifilar concentric coil in **Fig. 3F**.

[0052] One practical coil and well suited use as an inductive element 23 is the so-called bifilar configuration that can be utilized as a self-balanced inductive element due to the inter-winding stray capacitance, as shown in **Figs. 4A-4D**. Geometry of the bifilar inductive element for the inductive element 23 eliminates substantially the need for the connecting impedances 24 and 25 due to inter-winding capacitance of the individual coils. Multiple segments each constituting full 360 degree loops are illustrated in **Figs. 4A-4D**. Partial (less-than-360 degree) loops, more-than-360 degree loops, and one or more than one loop may be employed for the inductive element 23. The cross-section of the conductor of the inductive element 23 may be rectangular or circular or any other cross-section with typical overall diameter in range from 2 mm to 10 mm.

[0053] The inductive element 23 of the support 20 illustrated in **Fig. 2** is an embodiment of a compact i-ESIC device 20 with the inductive element 23 in a form of a single three turn coil integrated into the base-plate of the ESC or central portion 21. **Fig. 5A** illustrates an inductive element 23 made of two superimposed single turn coils. **Fig. 5C** is a simulation of time-averaged RF electromagnetic energy and **Fig. 5B** is a graph of RF power density delivered into the plasma 15, both in the absence of a Faraday shield 28. The annular distribution is typical for the i-ESICs described herein.

[0054] **Fig. 6A-6B** show an inductive element 23 made of three single-turn coils, with the impedances 24 and 25 omitted for convenience. **Fig. 6C** is a graph of simulation results of the distribution of time-averaged RF electromagnetic energy from and RF power density delivered into plasma 15. **Fig. 6D** is a diagram of a Faraday shield 28 with radial slots 29. A graph of the distribution of the RF power density through the shield of **Fig. 6D** is illustrated in **Fig. 6E**.

[0055] **Fig. 7** is a disassembled perspective view of an alternative embodiment of the wafer support of **Figs. 1** and **2** that employs a segmented peripheral source 50 for providing the inductive element 23. Segmented peripheral ICP sources are more particularly described in copending U.S. Patent Application Serial No. \_\_\_\_\_, Express Mail No. EV354971157US, filed on even date herewith, by the inventor hereof, and hereby expressly incorporated by reference herein in its entirety. The source 50 includes a segmented antenna which forms the inductive element 23, which is mounted in a congruent insulating plate 56 that separates the inductive device 23 from the chamber wall 12 and other conductive components of the chamber. The element 23 has terminals 51,52 that may respectively connect the inductor 23 in series between the impedances 24 and 25 (not shown in **Fig. 7**) and the ESC 21. An annular, segmented, slotted Faraday shield 53 is provided to serve as the shield 28 over the inductor 23. An insulator 54 may be provided between the shield 54 and the inductor 23. Otherwise, the inductor 23 of the source 50 may be connected in the various ways set forth above for the other inductor configurations. The embodiment of **Fig. 7** combines the features of the integrated, electrostatic, inductively-coupled wafer support (i-ESIC) 20 and the segmented peripheral ionization source of the incorporated patent application.

[0056] The invention has been described in the context of exemplary embodiments. Those skilled in the art will appreciate that additions, deletions and modifications to the features described herein may be made without departing from the principles of the present invention. Accordingly, the following is claimed: